

CMSC B240 Computer Organization - Spring 2024
Lab Activity #4: Combinational Logic Circuits

Question #1

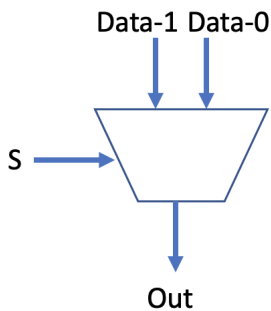
Recall that a **multiplexer**, or “mux”, is a circuit that has 2^N data input lines, and uses the value represented by the N select lines to choose which data line to produce as its single output.

Assume you have a 2-way mux (i.e., a mux with two data lines, one select line, and one output) as an individual component. First, complete the table with the output for each input combination:

| Data-1 | Data-0 | Select | Out |
|--------|--------|--------|-----|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

How could you combine some number of 2-way muxes to create a **4-way mux**, i.e. one that has four data lines, two select lines, and one output?

Using a representation like this for your 2-way mux:



draw the circuit diagram for a 4-way mux. You may use NOT, OR, and AND gates as needed, but should attempt to design this circuit using only a combination of 2-way muxes.

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Question #2

A **demultiplexer**, or “demux”, is similar to a mux but works in the opposite direction: it has one data line, N select lines, and 2^N output lines: the selected output line equals the data line, and the rest are 0.

Complete the truth table for a 2-way demux, i.e. a demux with $N = 2$.

| S-1 | S-0 | Data | Out-0 | Out-1 | Out-2 | Out-3 |
|-----|-----|------|-------|-------|-------|-------|
| 0 | 0 | 0 | | | | |
| 0 | 0 | 1 | | | | |
| 0 | 1 | 0 | | | | |
| 0 | 1 | 1 | | | | |
| 1 | 0 | 0 | | | | |
| 1 | 0 | 1 | | | | |
| 1 | 1 | 0 | | | | |
| 1 | 1 | 1 | | | | |

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Question #3

Consider a computer system that has a 32-bit address space and 2-byte addressability. How much **addressable memory** does this system have?

Question #4

Consider a computer system that has 8GB of addressable memory and a 32-bit address space, and assume each instruction is 16 bits long (remember, instructions are stored in memory along with data). How many **addresses** are required to hold one instruction in this system?

Question #5

Consider a memory system with the following design:

- When data is read from memory, it uses 16 multiplexers to get each of the bits
- Each of the multiplexers has 24 select lines
- The same 24 select lines are used to control each of the 16 multiplexers

How many **bytes** of memory can this system store in total?