LC-3 Specs & Main Components

Memory
- Addressability is 16 bits
- Address space is $2^{16} = 65,536$
- MAR, MDR

CPU
- ALU Word length is 16 bits
- ALU can perform ADD, AND, and NOT
- Has 8 16-bit registers (R0, R1, ..., R7)
- Has three 1-bit registers (N, Z, P)
- CU has a CLK
- CU has an Instruction Register (IR)
- CU has a Program Counter (PC)

Input
- Keyboard
- Has KBDR and KBSR

Output
- Monitor
- Has DDR and DSR

The Instruction Set Architecture (ISA)

Defines the CPU's machine-level instructions and their encoding.

Note: In a von Neumann computer the instructions and data are stored in the memory.
11 Instruction Set Architecture (ISA)

Tuesday, March 23, 2021  9:30 PM

1. What instruction is it? What should the CPU do?
2. How is it encoded/decoded.

Instruction Structure

Encoding is done by the CPU designer.
Every instruction has 2 parts:

- opcode
- operands (or more operands)

LC-3: 4-bits

3 types of instructions:

1. Operate
   operate on data
   \[ R_2 \leftarrow R_1 + R_2 \]
   dest \( R \)  src\( R \)  src\( R \)
   registers

   LC-3 has 3: ADD, AND, NOT
   \[ R_x \leftarrow R_1 + \#15 \]
   dest \( R \)  src\( R \)  add \( \#15 \)
   immediate value

2. Data Movement
   CPU \( \leftrightarrow \) Memory
   LC-3 has 6 instructions
   e.g.
   load the contents of a memory location into \( R \)
   load contents of \( R \) into a memory location
   \[ R[i] \leftarrow M[\text{address}] \]
   \[ M[\text{address}] \leftarrow R[i] \]

3. Control
   by default execution is sequential
   e.g. branch

4. STOP/HALT

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

opcode \( \leftarrow \) operands
Each instruction is 16-bits (1 word)
Bits 15:12 specify opcode

ADD

ADD

AND

LOAD

BRANCH

HALT
1. **Fetch**
   \[ IR \leftarrow M[PC] \]

2. **Evaluate Address**
   - Only needed when \( M \) is accessed
   - \( R2 \leftarrow M[PC+1] \)
   - Not needed for \( R2 \leftarrow R2 + R3 \)

3. **Fetch operands**
   \[ MDR \leftarrow M[PC+1] \]
   \[ R2 \leftarrow MDR \]

4. **Execute**
   - **ALU** does the instruction
   \[ R2 \leftarrow R2 + R3 \]
   \[ R2 \leftarrow R2 + \text{SEXT}(\#5) \]

   **Store Result**